IN THE CLAIMS

1. (Original) A method of manufacturing a semiconductor device on a semiconductor substrate, comprising:

forming a gate dielectric on the semiconductor substrate;

forming a gate stack overlying the gate dielectric, the gate stack having a sidewall, wherein the gate stack comprises a conductive layer and a capping nitride layer overlying the conductive layer;

selectively depositing a liner over the gate stack such that the liner is deposited on the capping nitride layer at a rate lower than the rate of deposition on the conductive layer, so that the liner is thinner on the capping nitride layer than on the conductive layer; and

forming a nitride spacer over the liner.

2. (Original) The method of claim 1, wherein said forming a nitride spacer comprises:

forming a layer of nitride spacer material conformally over the liner; and

etching back the layer of nitride spacer material.

3. (Original) The method of claim 1, wherein the liner is deposited on the capping nitride layer at a rate approximately one-fifth the rate of deposition on the conductive layer.

4. (Original) The method of claim 1, wherein the liner is deposited selectively on the conductive layer in a thickness at least twice a thickness of deposition of the capping layer.

5. (Original) The method of claim 1, wherein said liner is formed of oxide.

6-20. (cancelled)

21. (previously added) The method of claim 1, wherein selectively depositing a liner comprises using surface characteristics of the gate stack.

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22. (previously added) A method of manufacturing a semiconductor device on a semiconductor substrate, comprising:

forming at least two adjacent gate stacks over the substrate, the adjacent gate stacks each having a sidewall opposing each other,

wherein each of the gate stacks comprises a conductive layer and a capping nitride layer overlying the conductive layer;

selectively depositing a liner over the gate stacks, so that the liner is thicker on the conductive layer than on the capping nitride layer; and

forming adjacent at least two nitride spacers on the liner, overlying the opposing sidewalls,

wherein the liner is deposited over the capping nitride layer at a rate lower than the rate of deposition on the conductive layer.

23. (previously added) The method of claim 22, wherein the liner is deposited on the capping nitride layer at a rate approximately one-fifth the rate of deposition on the conductive layer.

24. (previously added) The method of claim 22, wherein the liner is deposited selectively on the conductive layer in a thickness at least twice a thickness of deposition of the capping layer.

25. (previously added) The method of claim 22, wherein said forming adjacent nitride spacers comprises:

forming a layer of nitride spacer material conformally over the liner; and

etching back the layer of nitride spacer material.

26. (previously added) The method of claim 22, wherein the adjacent nitride spacers have top, middle, and bottom spaces therebetween, and wherein the bottom space is substantially shorter than the middle space.

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